

**In the Specification:**

**Please replace the Title of the Invention with the following:**

CDD Array

**Please AMEND the paragraph beginning at page 1, line 11, with the following amended paragraph:**

An image reader, which scans an original in the main scanning direction with a line image sensor (to be referred to as a CCD hereinafter), and at the same time, relatively scans ~~the CCD or~~ the original in the sub-scanning direction (a direction perpendicular to the CCD element arrays), thereby obtaining two-dimensional image information, is known. An example of this type of image reader uses a technique of improving the image read resolution by increasing the number of CCD elements and arranging them in a staggered pattern (refer to Japanese Patent Laid-Open No. 57-141178, Japanese Patent Publication No. 59-6666, and the like).

**Please AMEND the paragraph beginning at page 14, line 19, with the following amended paragraph:**

As shown in Figs. 1 and 2, the CCD can selectively output only the image data read by either the odd or even photodiode arrays. And then, even if the frequencies of the transfer clocks  $\phi 1$  and  $\phi 2$  and reset clock RS are increased twice those in the prior art, sufficient output time can be ensured for image data in each element which is outputted from the output buffer. More specifically, as compared with the case shown in Fig. 21 in which image data in all the elements are outputted from the CCD and thinned out by the S/H circuit, with the operation

shown in Figs. 1 and 2, the interval between the instant at which image data is outputted from the shift register to the output buffer and the instant at which the image data is reset is long, and hence the precision of outputting data from the CCD (output buffer) improves.

**Please AMEND the paragraph beginning at page 21, line 1, with the following amended paragraph:**

Fig.. 12 shows a preferable embodiment of the 1/4-resolution read mode. In this preferable embodiment clocks  $\phi 1$ ,  $\phi 2$ ,  $\phi 3$ , and RS is driven to ~~exchange~~ change potential state in a cycle of  $Tb2 \rightarrow Tb3 \rightarrow Tb5 \rightarrow Tb6 \rightarrow Tb2 \rightarrow Tb3 \rightarrow \dots$ , in FIG. 9, with an omission of an illustration concerning the timings  $Tb1$ ,  $Tb4$ ,  $Tb7$ , and  $Tb8$ , so that data can be efficiently shifted and the precision in outputting data from the output buffer can be improved when compared with Fig. 9.